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2811

AMENDMENT TRANSMITTAL LETTER (Large Entity) Applicant(s): YOSHITAKE HORIE	Docket No. KIX0154-US

Serial No.	Filing Date	Examiner	Group Art Unit
09/917,945	July 31, 2001	Q. D. Vu	2811

Invention: METHOD OF MAKING WIRELESS SEMICONDUCTOR DEVICE, AND LEADFRAME USED THEREFOR

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST # PREV. PAID FOR		NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE
TOTAL CLAIMS	15	-	20	=	0	x $18.00	$0.00
INDEP. CLAIMS	3	-	3	=	0	x $84.00	$0.00
Multiple Dependent Claims (check if applicable) ☐							$0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT							$0.00

☒ No additional fee is required for amendment.

☐ Please charge Deposit Account No. in the amount of
A duplicate copy of this sheet is enclosed.

☐ A check in the amount of to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. **50-1390.**
A duplicate copy of this sheet is enclosed.

☒ Any additional filing fees required under 37 C.F.R. 1.16.

☒ Any patent application processing fees under 37 CFR 1.17.

Dated: **December 8, 2003**

Signature

Michael D. Bednarek
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CUSTOMER NO. 28970

I certify that this document and fee is being deposited on with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

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cc:

KIX0154-US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	
YOSHITAKA HORIE	
Serial No.: 09/917,945	Art Unit: 2811
Filed: July 31, 2001	Examiner:
For: METHOD OF MAKING WIRELESS SEMICONDUCTOR DEVICE, AND LEADFRAME USED THEREFOR	

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed on August 6, 2003, please amend the above-identified application as follows:

A Petition for One Month Extension of Time is being filed herewith, thereby extending the period for response to December 6, 2003. Any extension of time necessary to prevent abandonment is hereby requested, and any fee necessary for consideration of this response is hereby authorized to be charged to Deposit Account Number 50-1390.

Amendments to the Claims: reflected in the listing of claims that begins on page 2 of this paper.

Remarks: begin on page 4 of this paper.

This listing of claims replaces all prior versions, and listings, of claims in this application.

Listing of Claims:

1. (Currently Amended) A method of making a semiconductor device, the method comprising the steps of:

mounting a semiconductor chip on a lower conductor, with first solder material applied between the chip and the lower conductor;

positioning an upper conductor on the chip, with second solder material applied between the chip and the upper conductor;

heating up the first and the second solder materials beyond melting points of the respective solder materials; and

solidifying the first and the second solder materials;

wherein the lower conductor includes a die pad portion for mounting the semiconductor chip; and

wherein the first solder material has a melting temperature higher than that of the second solder material and is caused to solidify earlier than the second solder material in the solidifying step for securing the semiconductor chip on the die pad portion of the lower conductor before the upper conductor is fixedly connected to the semiconductor chip.

2. (Canceled)

3. (Original) The method according to claim 1, wherein the heating of the first solder material is terminated earlier than the heating of the second solder material.

4. (Original) The method according to claim 1, wherein the heating of the first and the second solder materials is performed by contacting the lower and the upper conductors with first and second heaters, respectively.

5. (Original) The method according to claim 1, wherein the semiconductor chip includes a flat lower electrode and a protruding upper electrode, the lower electrode being connected to the lower conductor, the upper electrode being connected to the upper conductor.

6. (Original) The method according to claim 1, further comprising the step of preparing a conductive frame which includes the lower and the upper conductors.

7. (Currently Amended) The method according to claim 6, wherein the lower conductor comprises ~~a die pad portion and~~ lower lead portions extending from the die pad portion~~, the semiconductor chip being mounted on the die pad portion~~.

8. (Original) The method according to claim 6, wherein the upper conductor comprises upper lead portions.

9. (Canceled)

10. (Canceled)

11. (Original) The method according to claim 6, further comprising the step of rotating the upper conductor about an axis relative to the lower conductor, so that the upper conductor comes into facing relation to the lower conductor.

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Original) The method according to claim 1, further comprising the step of preparing a conductive frame which includes a first conductive pattern and a second conductive pattern, the first conductive pattern including the lower conductor, the second conductive pattern including the upper conductor.

18. (Original) The method according to claim 17, wherein the lower conductor further comprises lower lead portions extending from the die pad portion.

19. (Original) The method according to claim 18, wherein the second conductive pattern comprises upper lead portions at least one of which is to be connected to the semiconductor chip as the upper conductor.

20. (Original) The method according to claim 19, further comprising the step of removing at least one of the lower and the upper lead portions from the frame.

21. (Original) The method according to clam 19, wherein the frame comprises first and second common bars parallel to each other, the upper lead portions being divided into first and second groups, the upper lead portions in the first group extending from the first common bar toward the second common bar, the upper lead portions in the second group extending from the second common bar toward the first common bar.

22. (Currently Amended) A method of making a semiconductor device, the method comprising the steps of:

mounting a semiconductor chip on a lower conductor, with first solder material applied between the chip and the lower conductor;

positioning an upper conductor on the chip, with second solder material applied between the chip and the upper conductor;

heating up the first and the second solder materials beyond melting points of the respective solder materials by contacting the lower and the upper conductors with first and second heaters, respectively; and

solidifying the first and the second solder materials;

wherein the first solder material is caused to solidify earlier than the second solder material in the solidifying step; and

wherein the heating of the first solder material is terminated earlier than the heating of the second solder material.

23. (Currently Amended) A method of making a semiconductor device, the method comprising the steps of:

mounting a semiconductor chip on a lower conductor, with first solder material applied between the chip and the lower conductor;

positioning an upper conductor on the chip with second solder material applied between the chip and the upper conductor;

heating up the first and the second solder materials beyond melting points of the respective solder materials; and

solidifying the first and the second solder materials;

wherein the first solder material is caused to solidify earlier than the second solder material in the solidifying step; and

wherein the heating of the first and the second solder materials is performed by contacting the lower and the upper conductors with first and second heaters, respectively.